

FIG. 1A

FIG. 1B

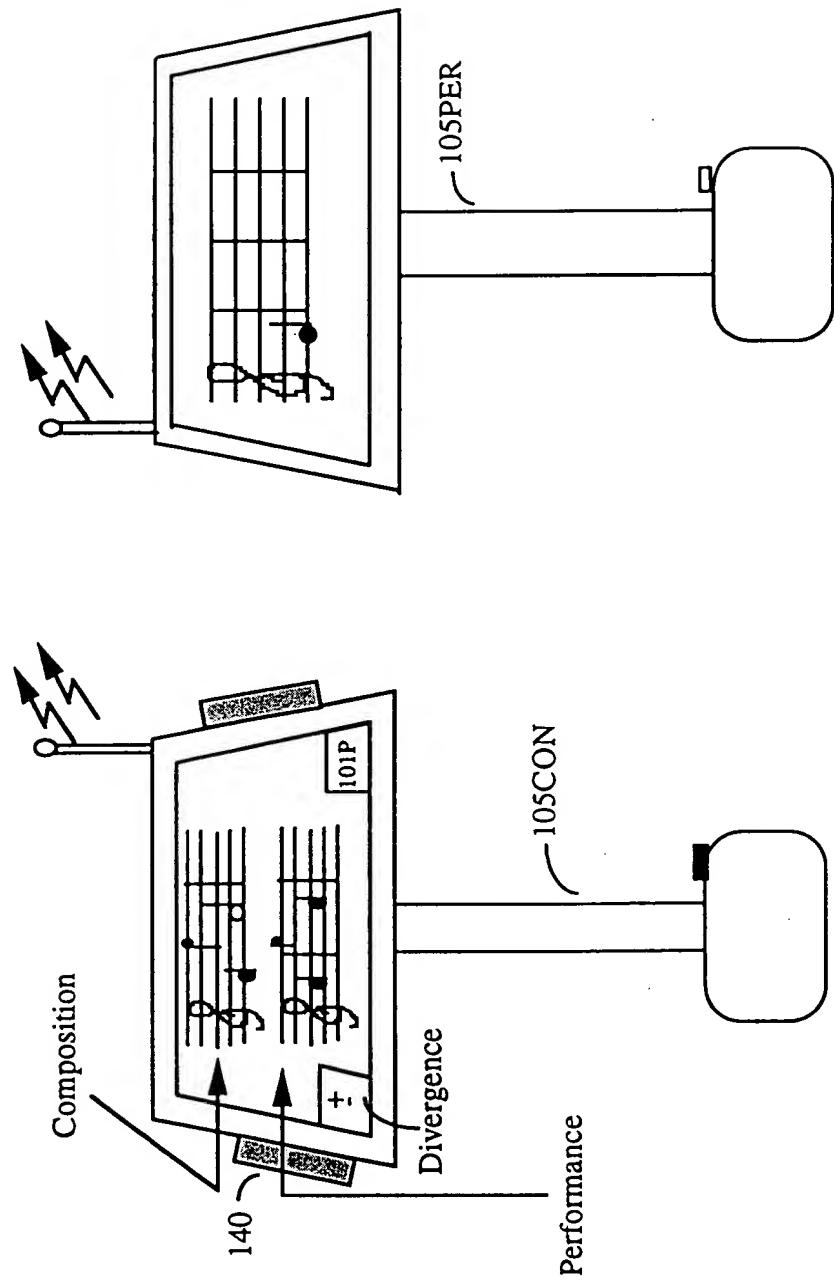
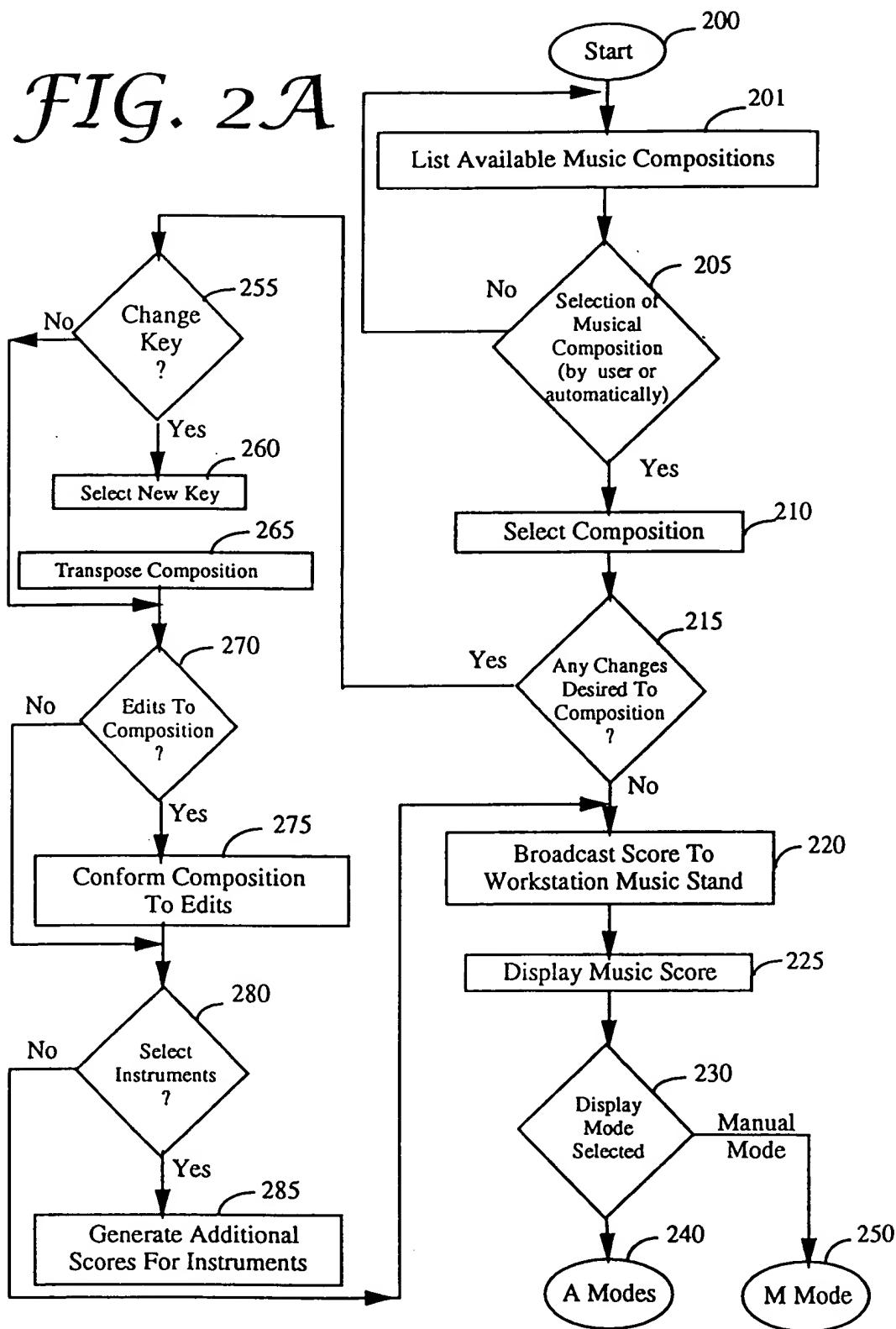


FIG. 2A



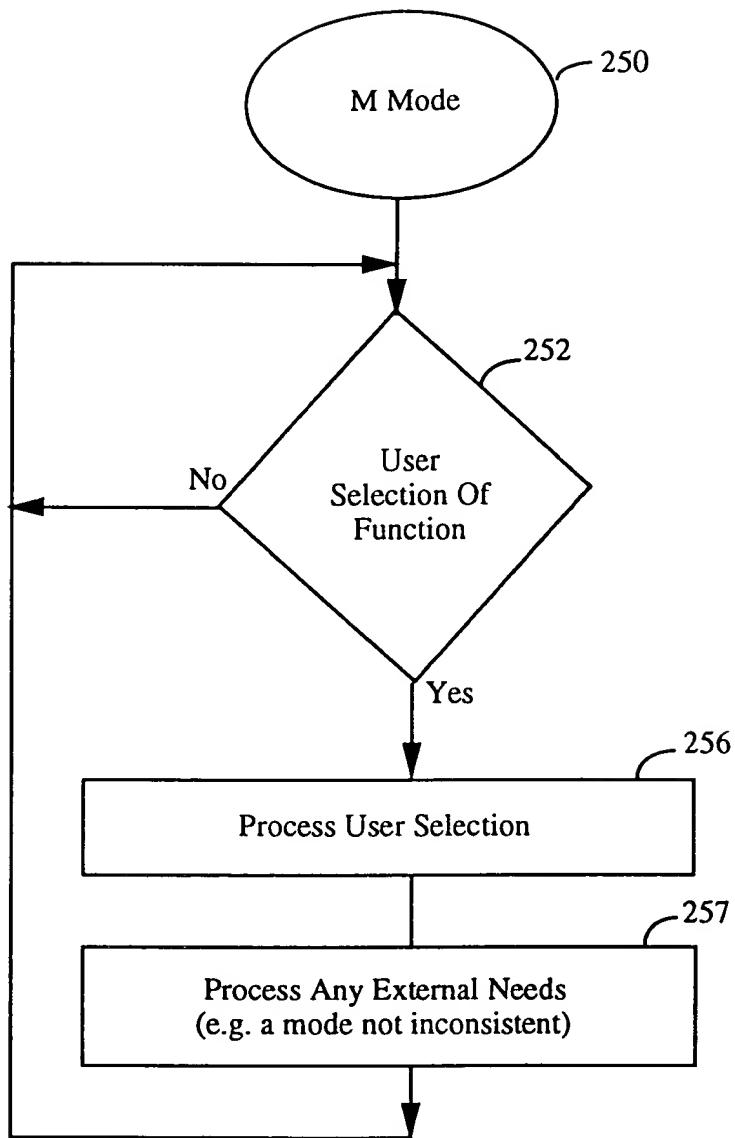


FIG. 2B

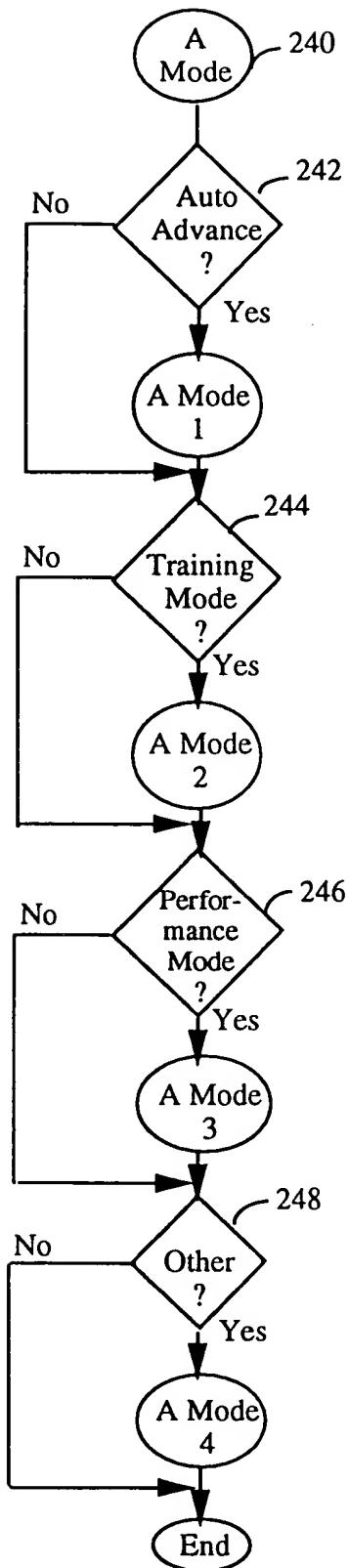


FIG. 2C

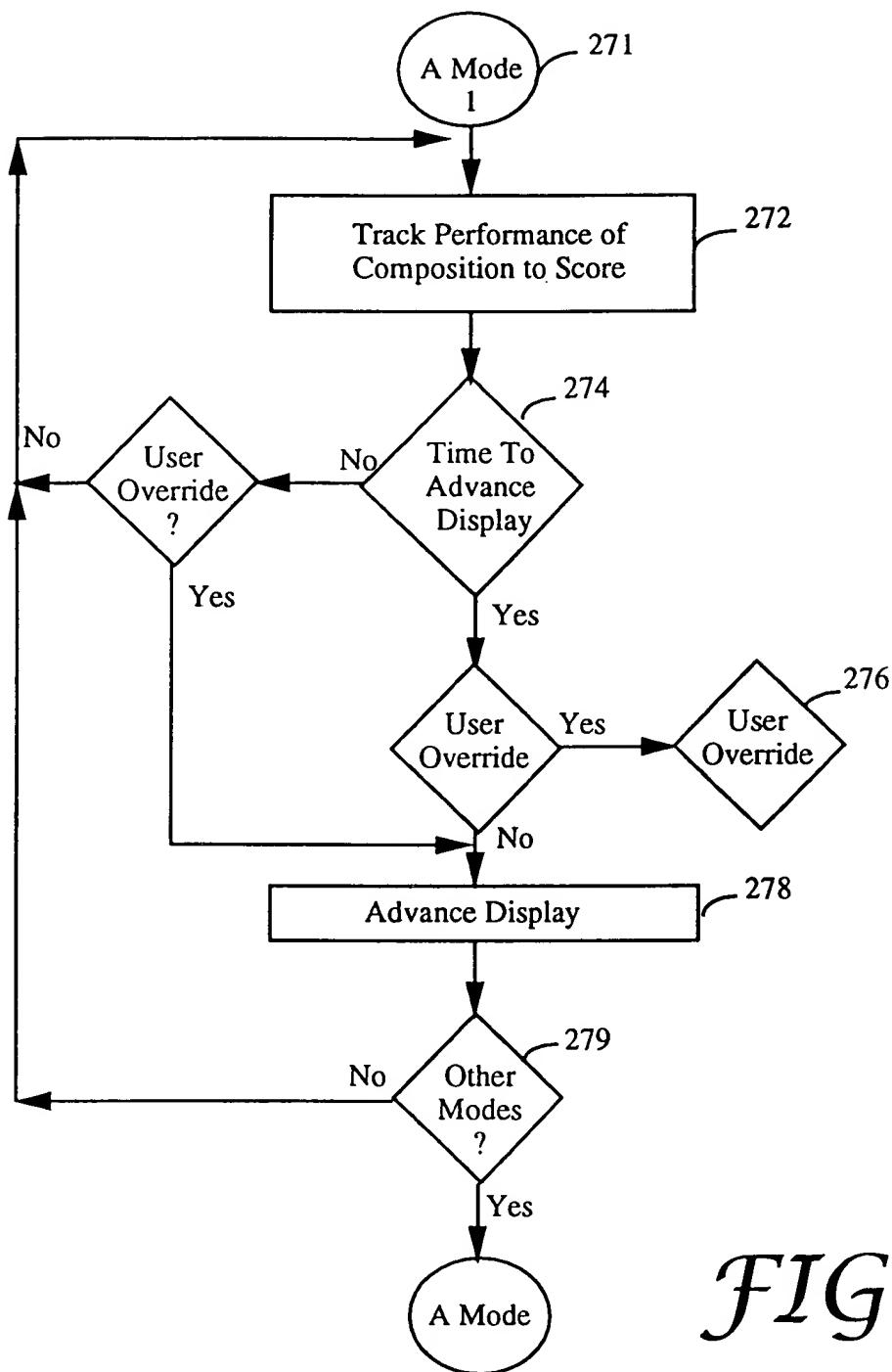


FIG. 2D

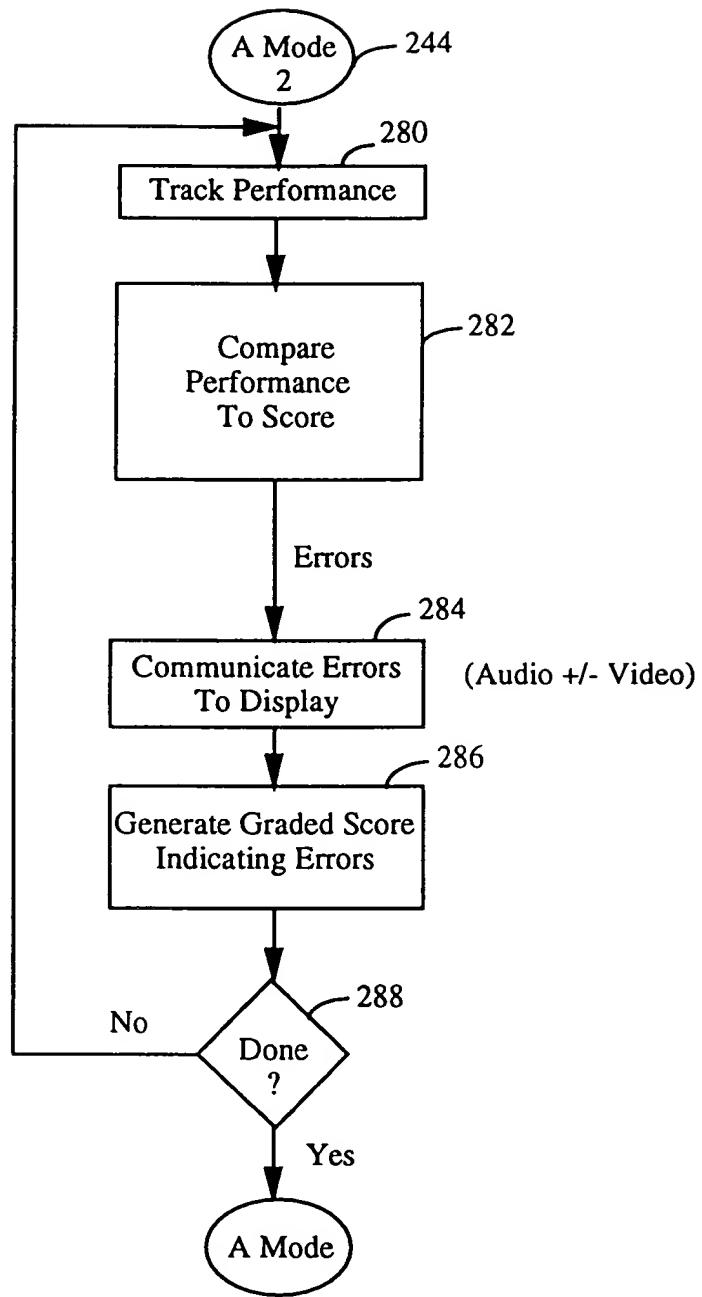


FIG. 2E

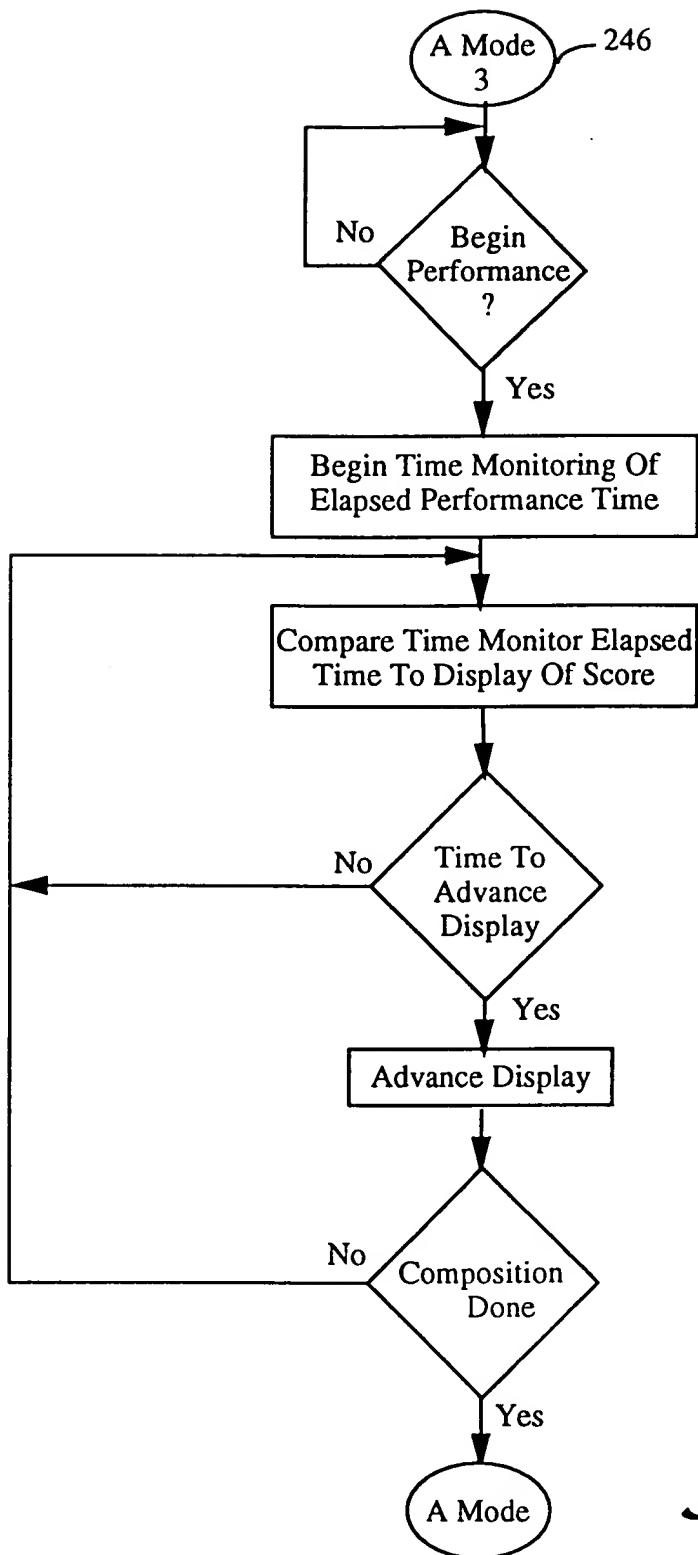
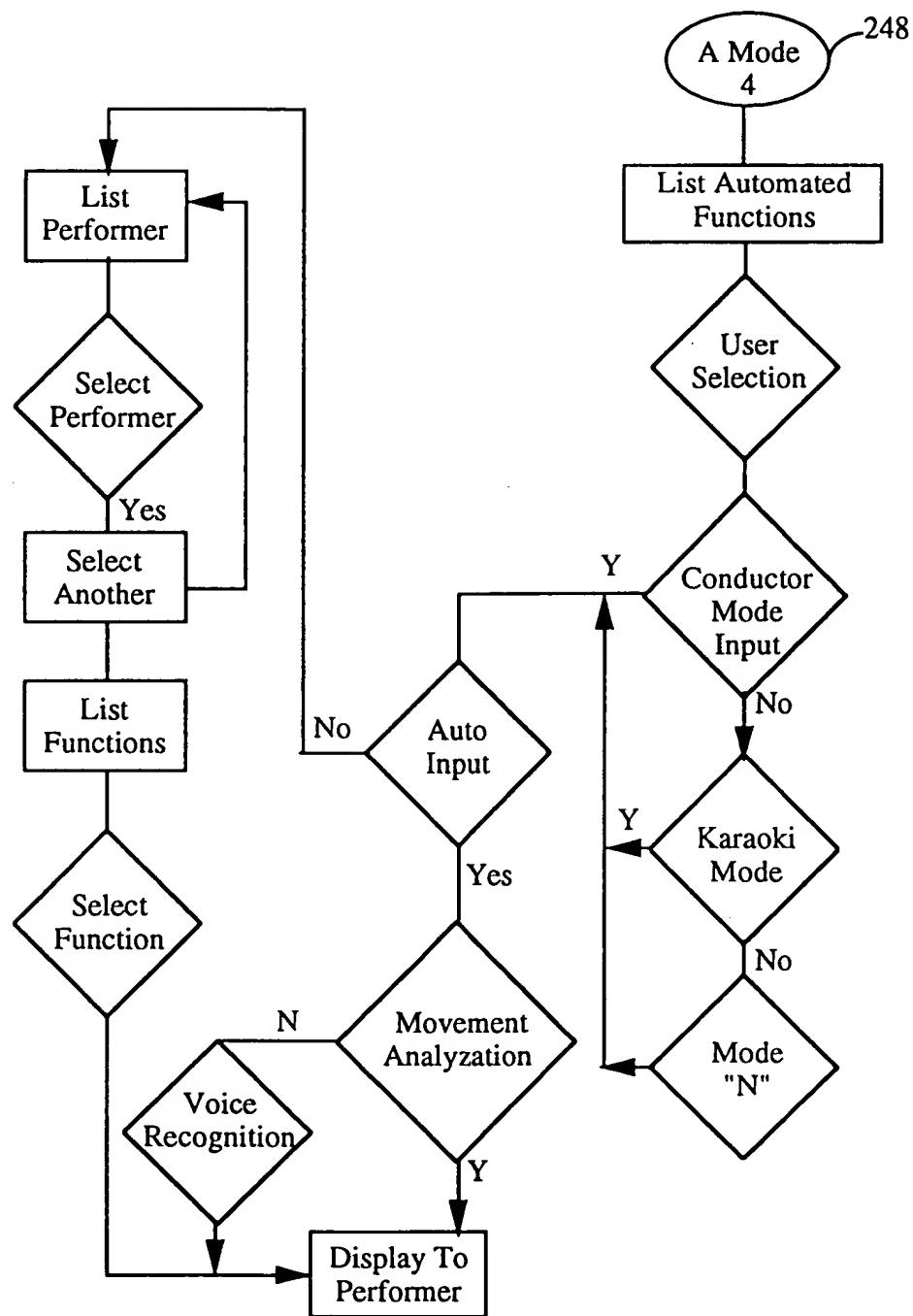


FIG. 2F

FIG. 2G

CONDUCTOR MODE



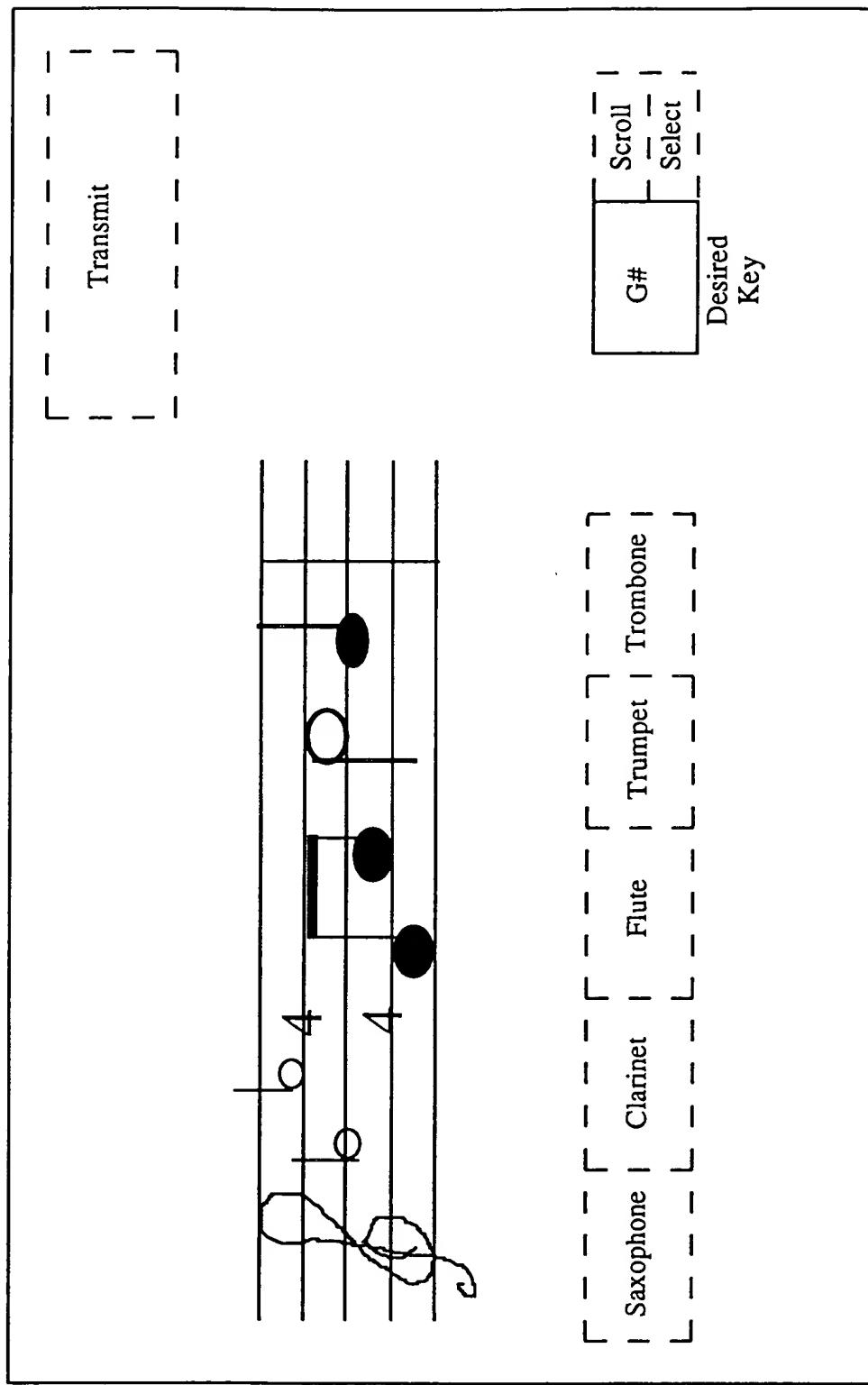
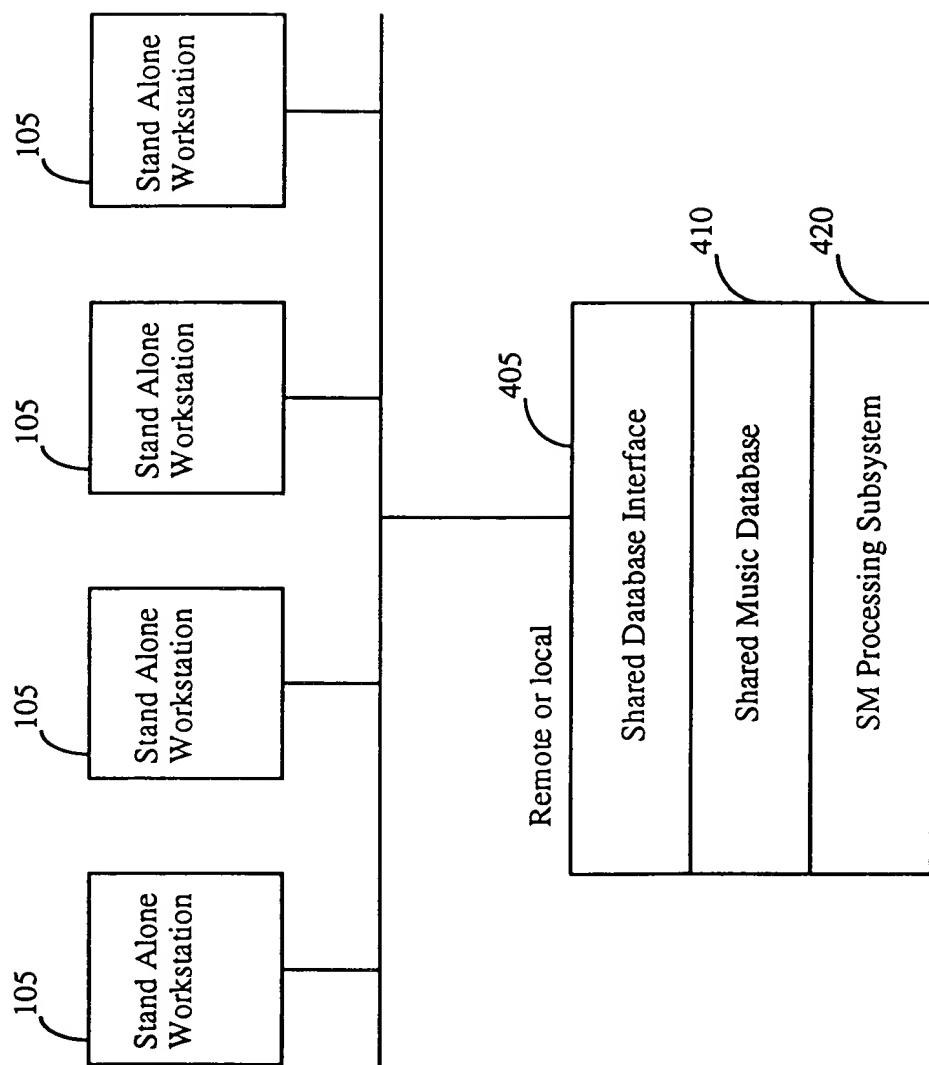


FIG. 3

FIG. 4



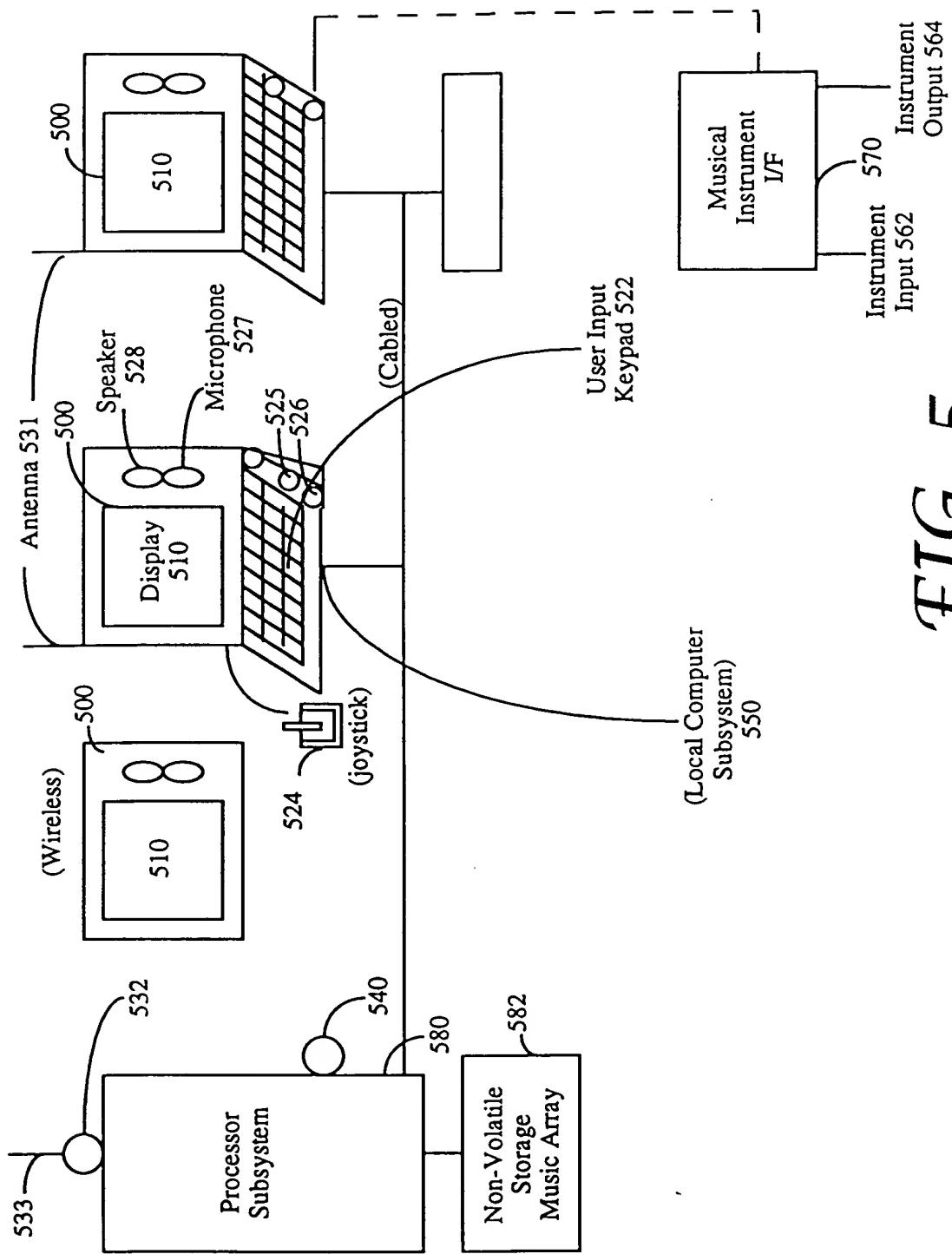


FIG. 5

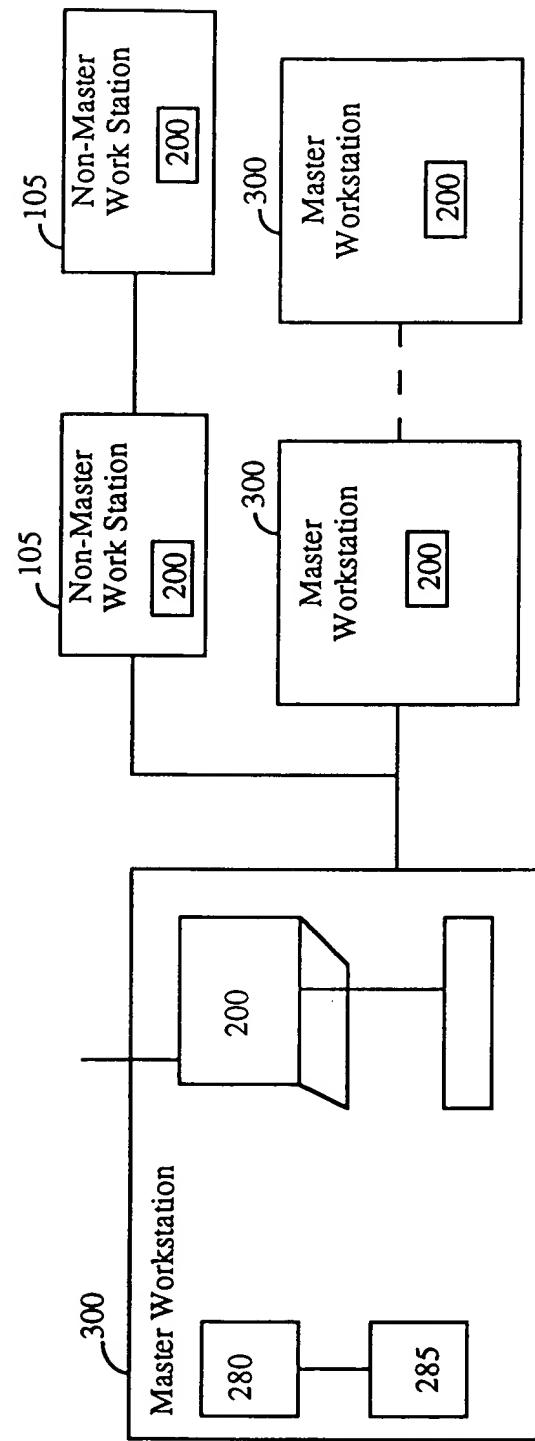
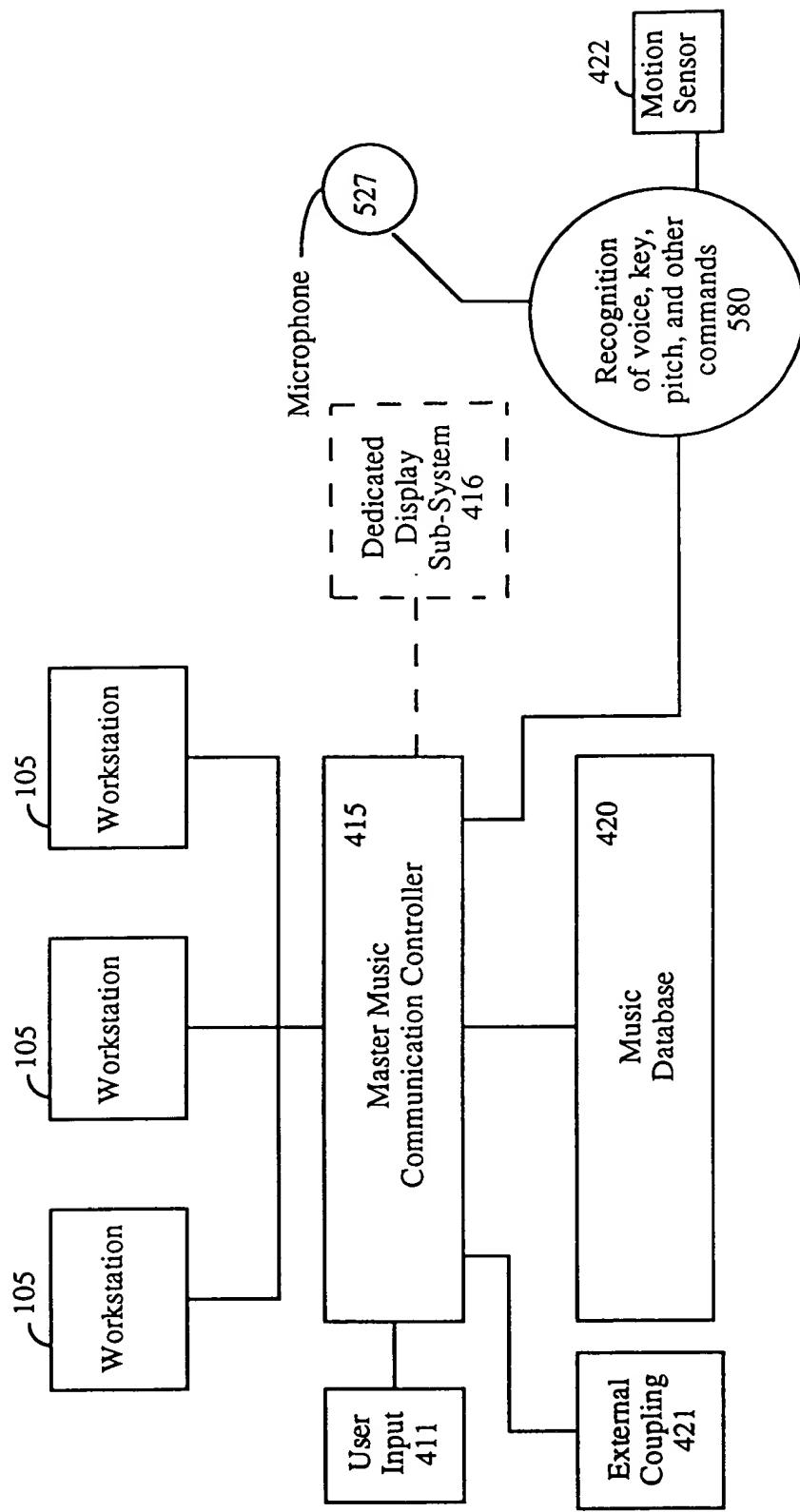


FIG. 6

FIG. 7



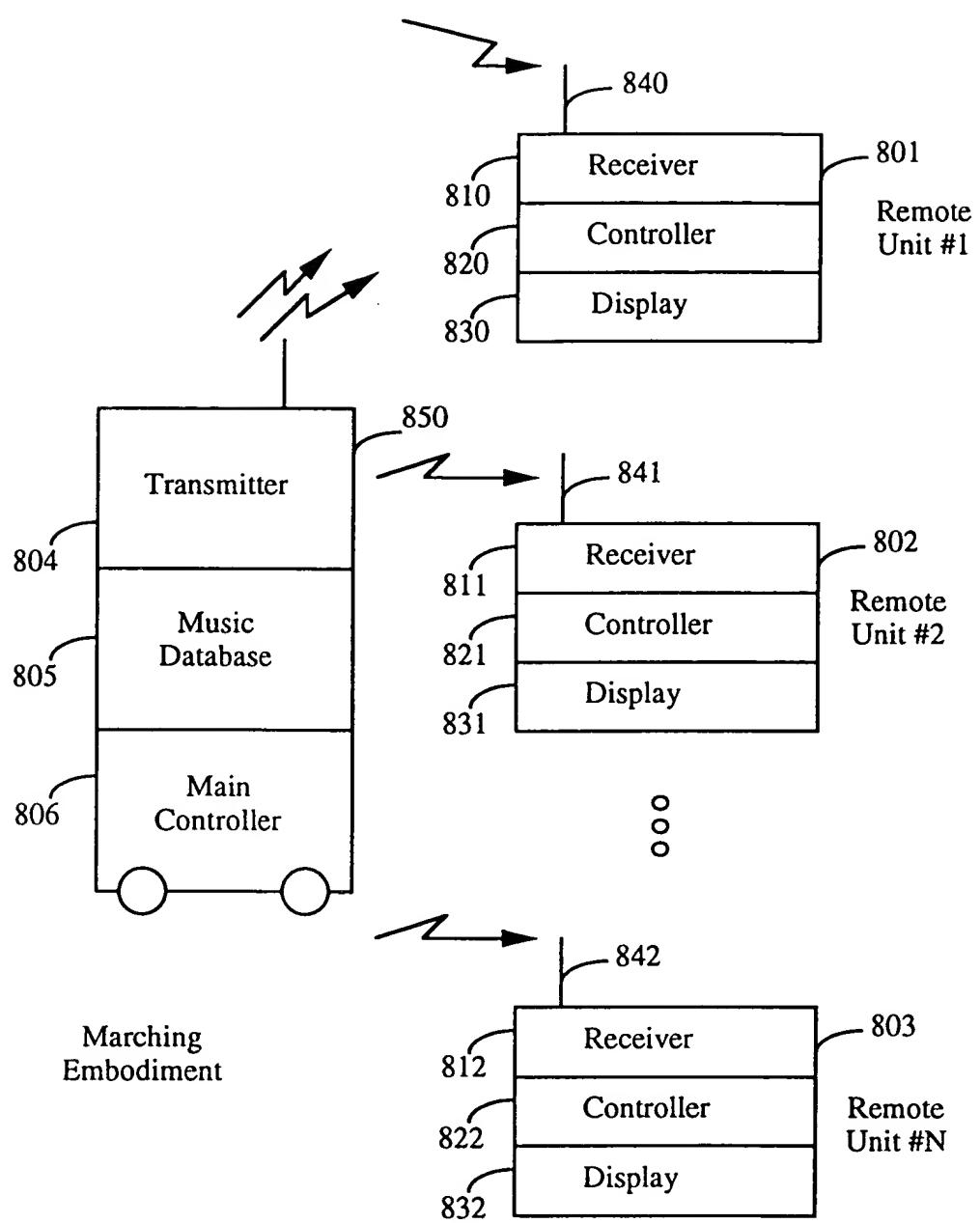


FIG. 8

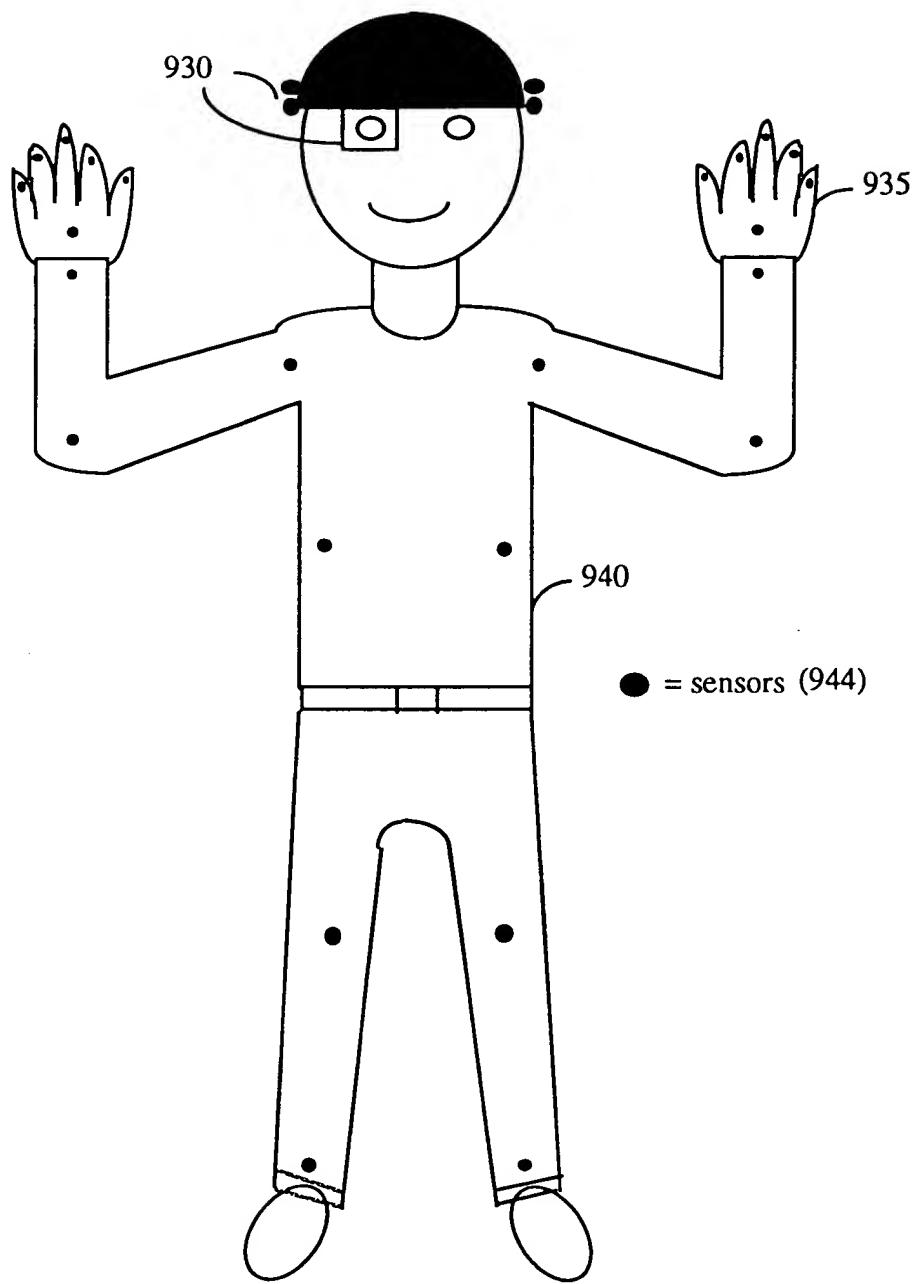


FIG. 9

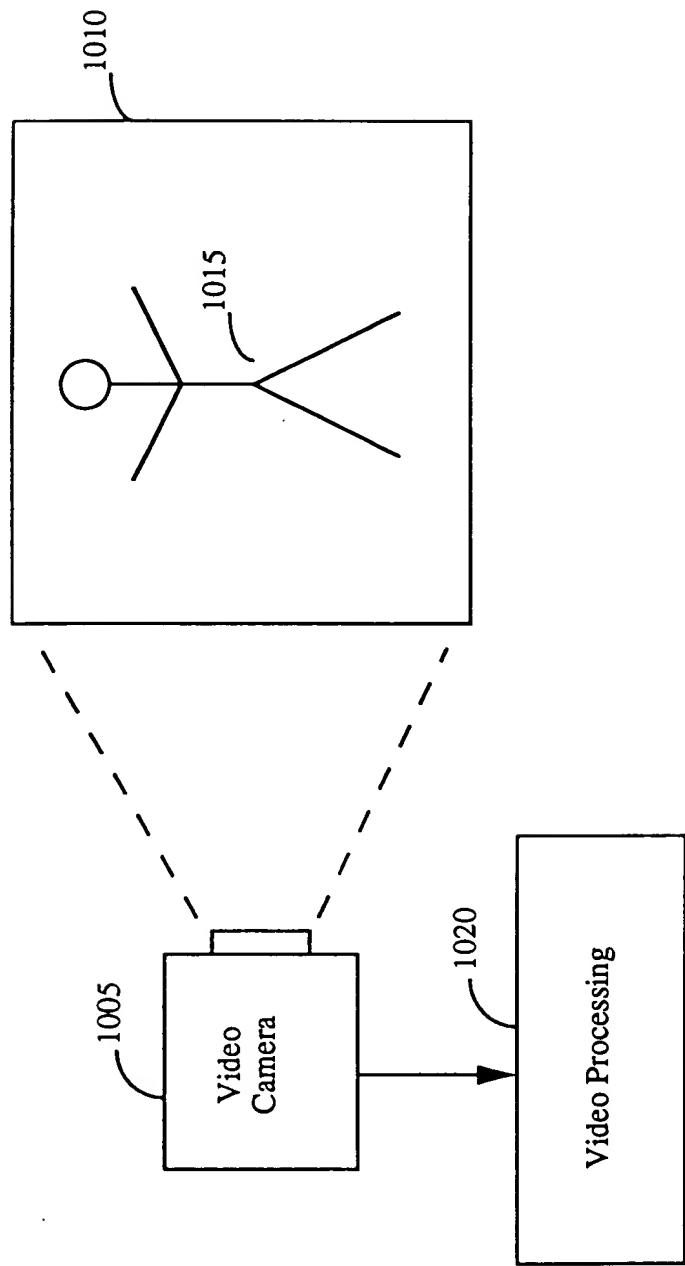


FIG. 10

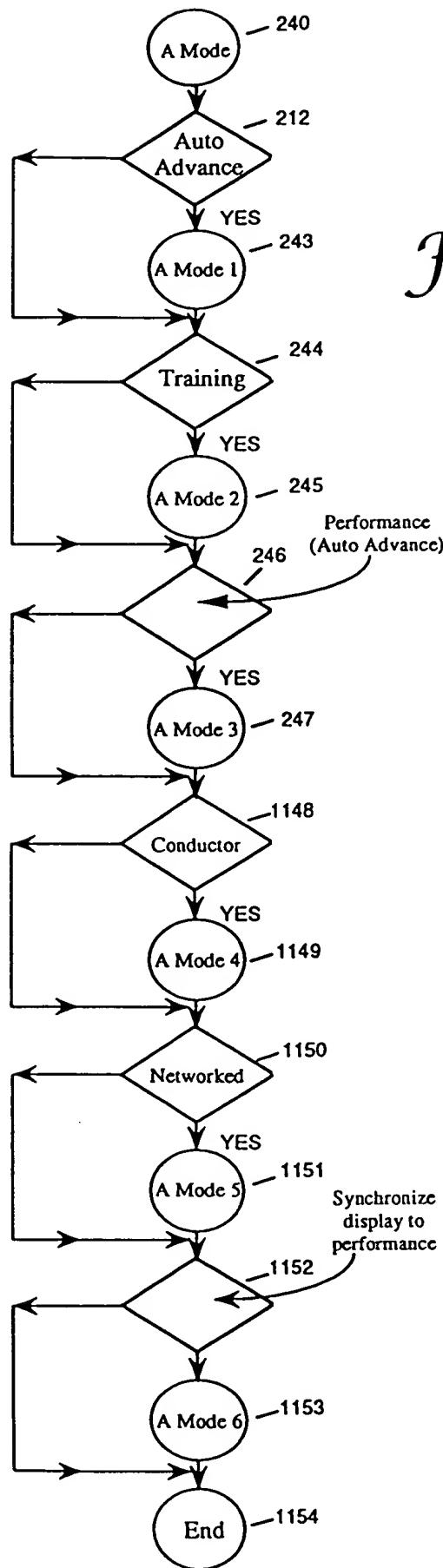
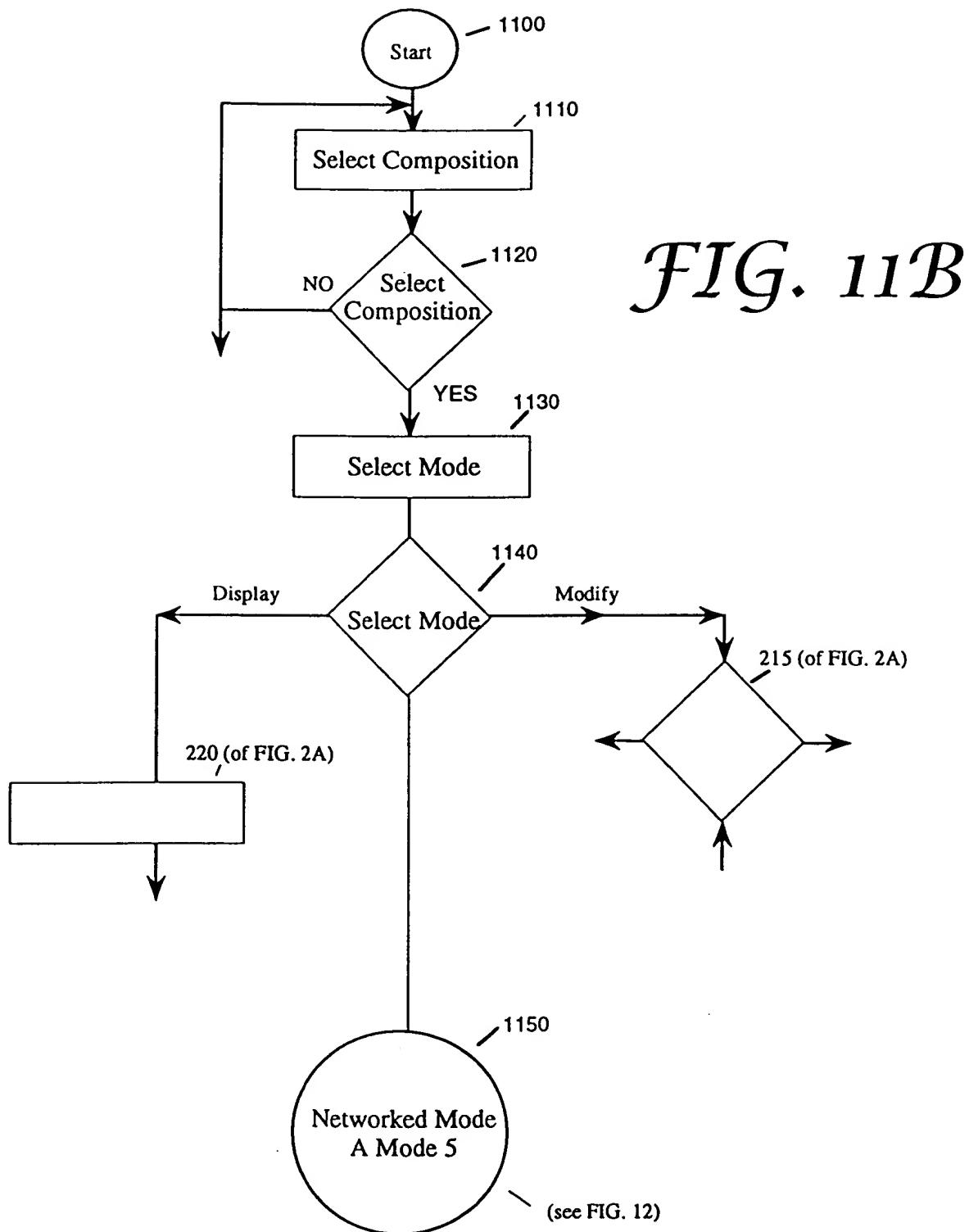


FIG. 11A



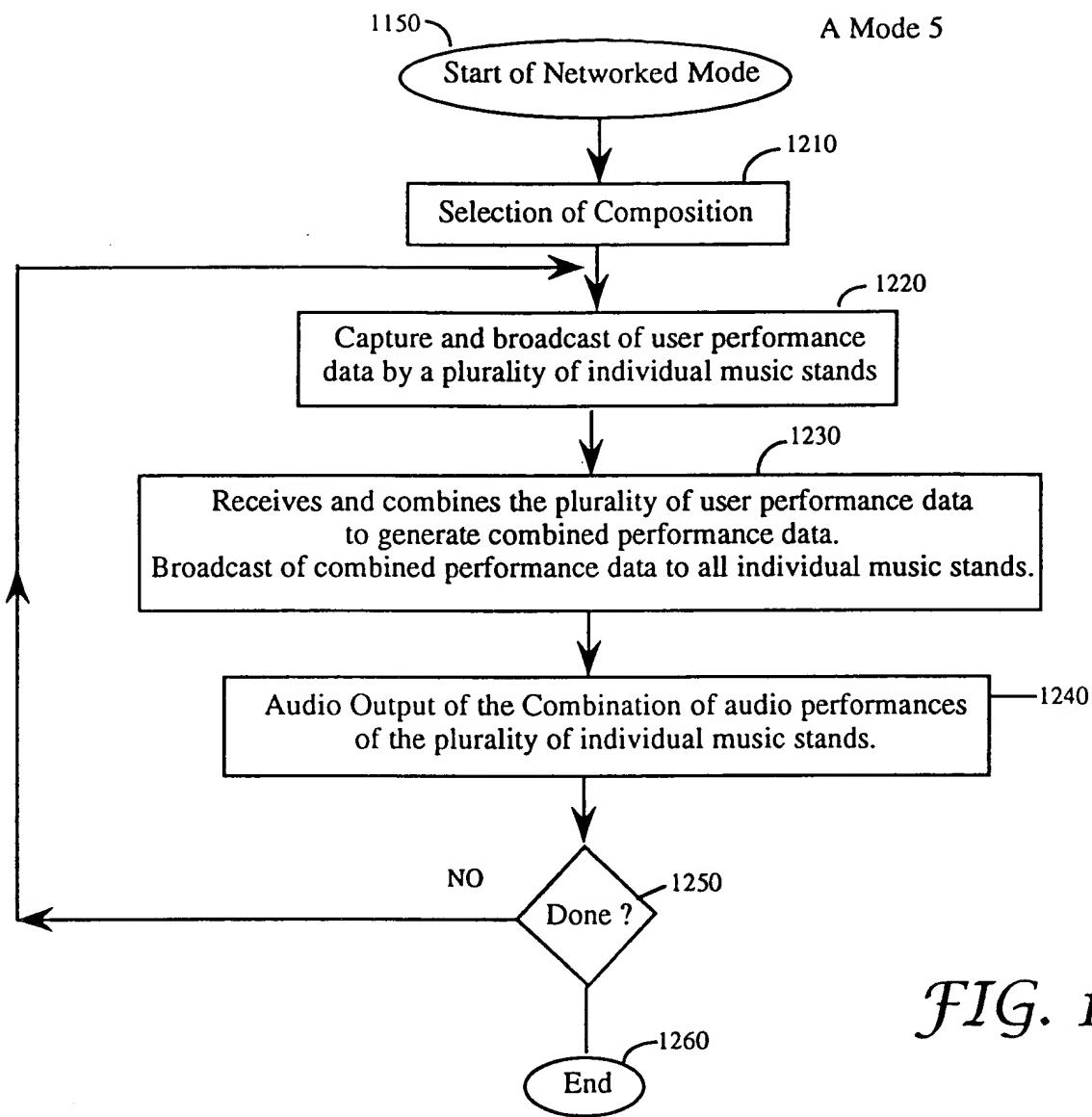


FIG. 13

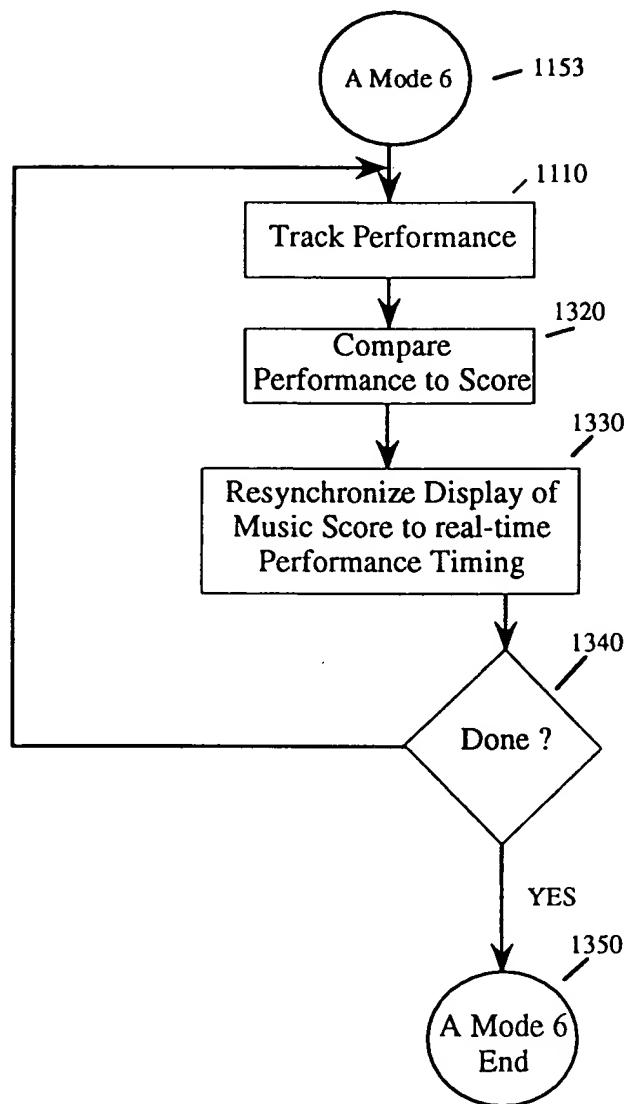
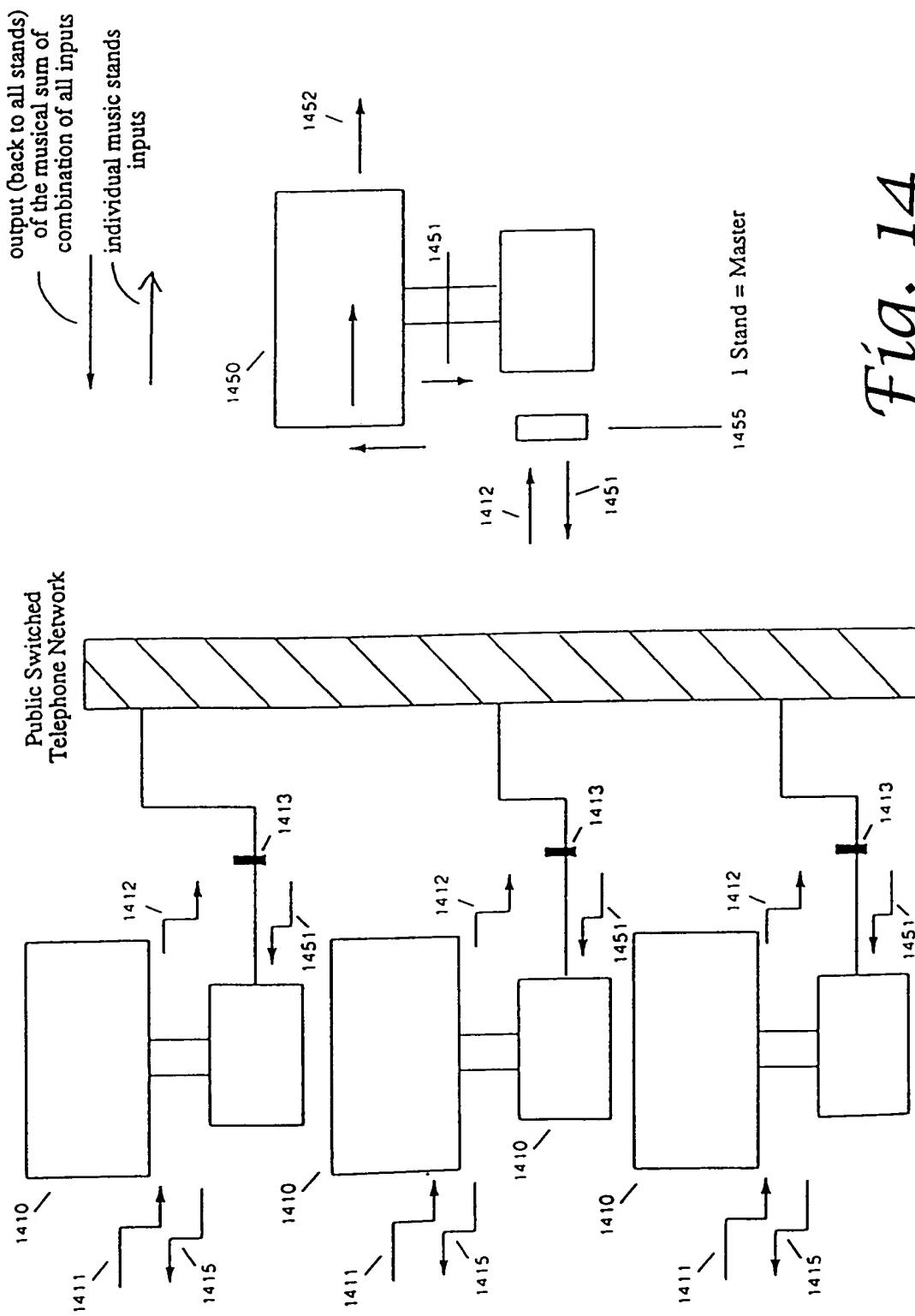


Fig. 14



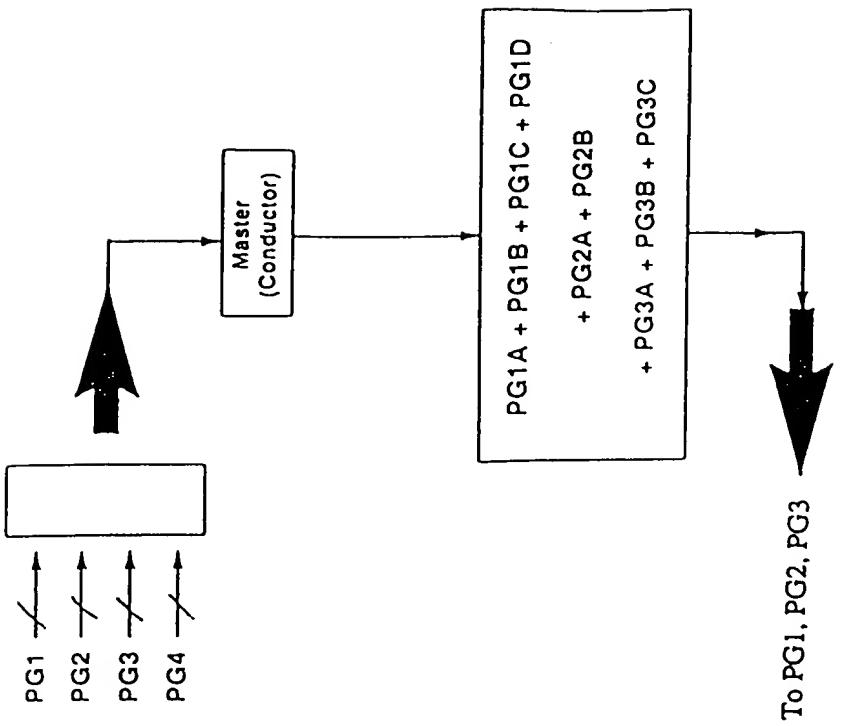
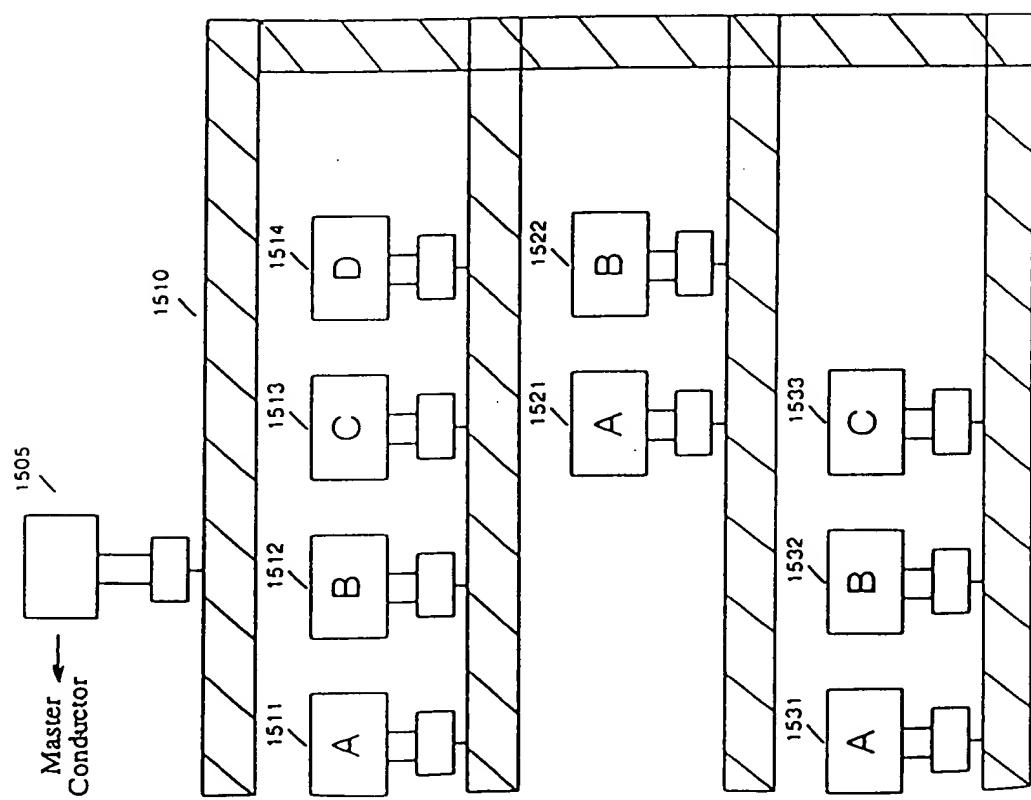
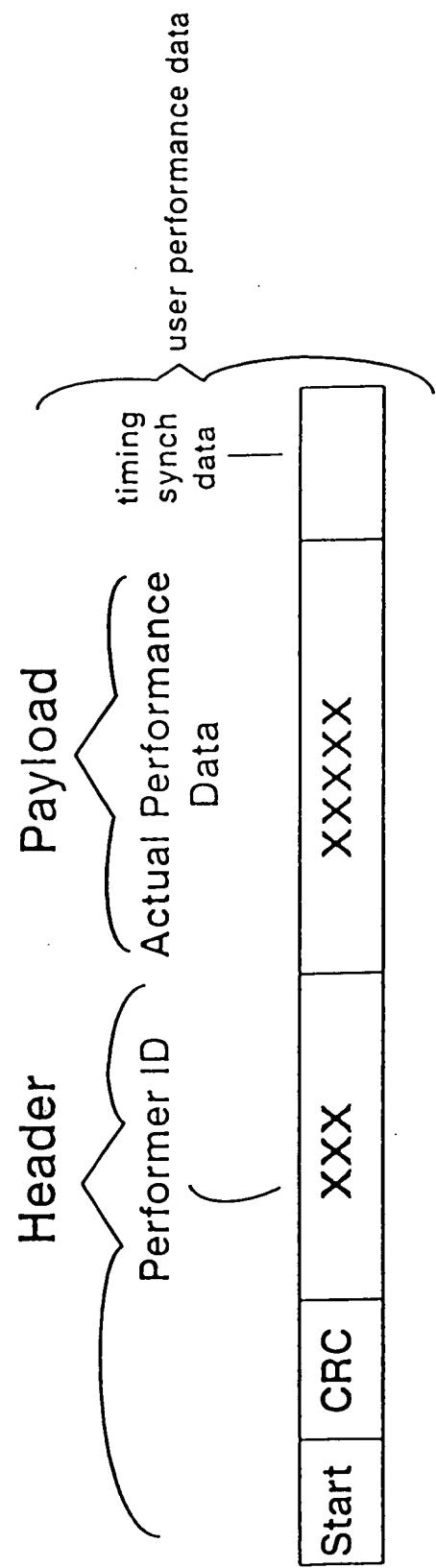


Fig. 15

Fig. 16



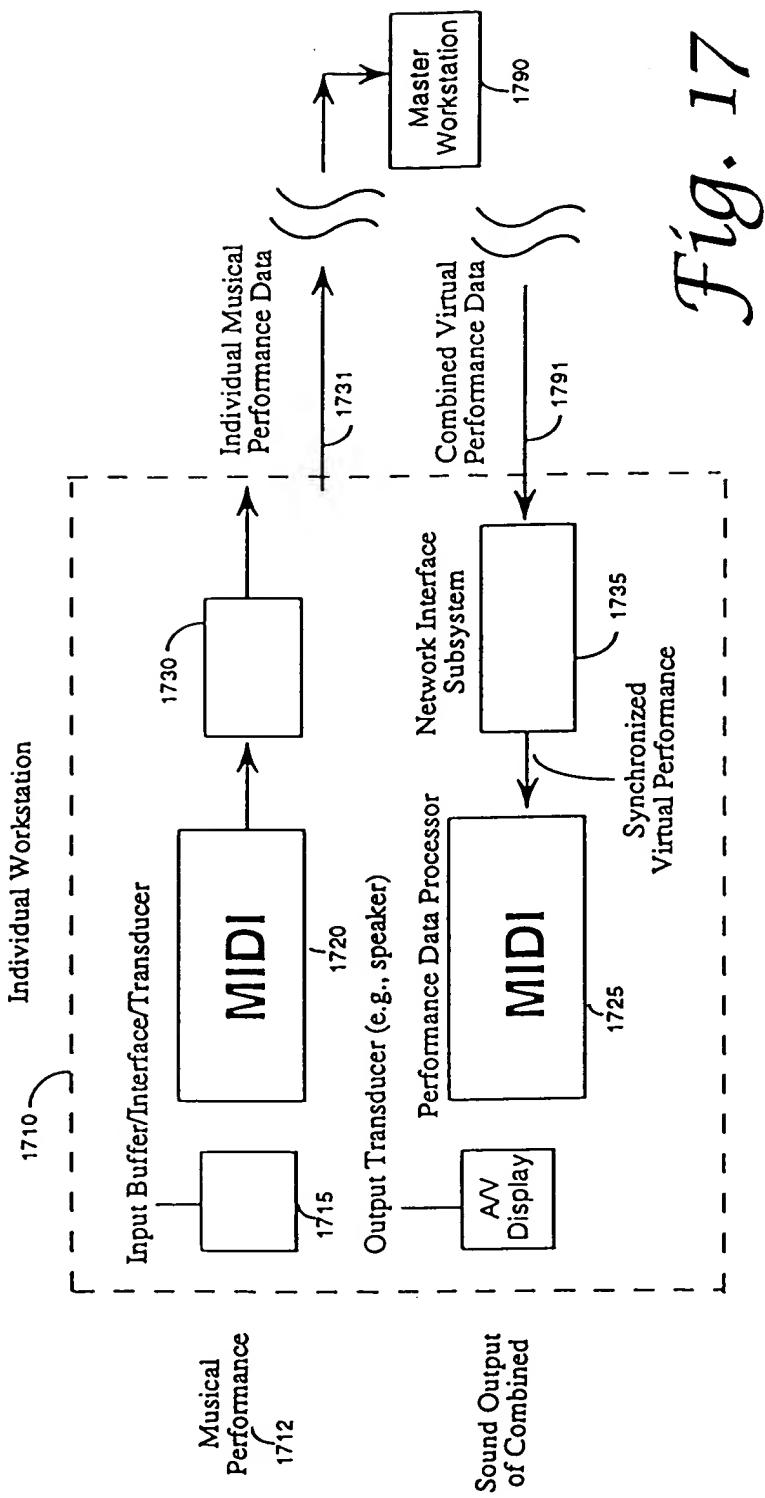


Fig. 17

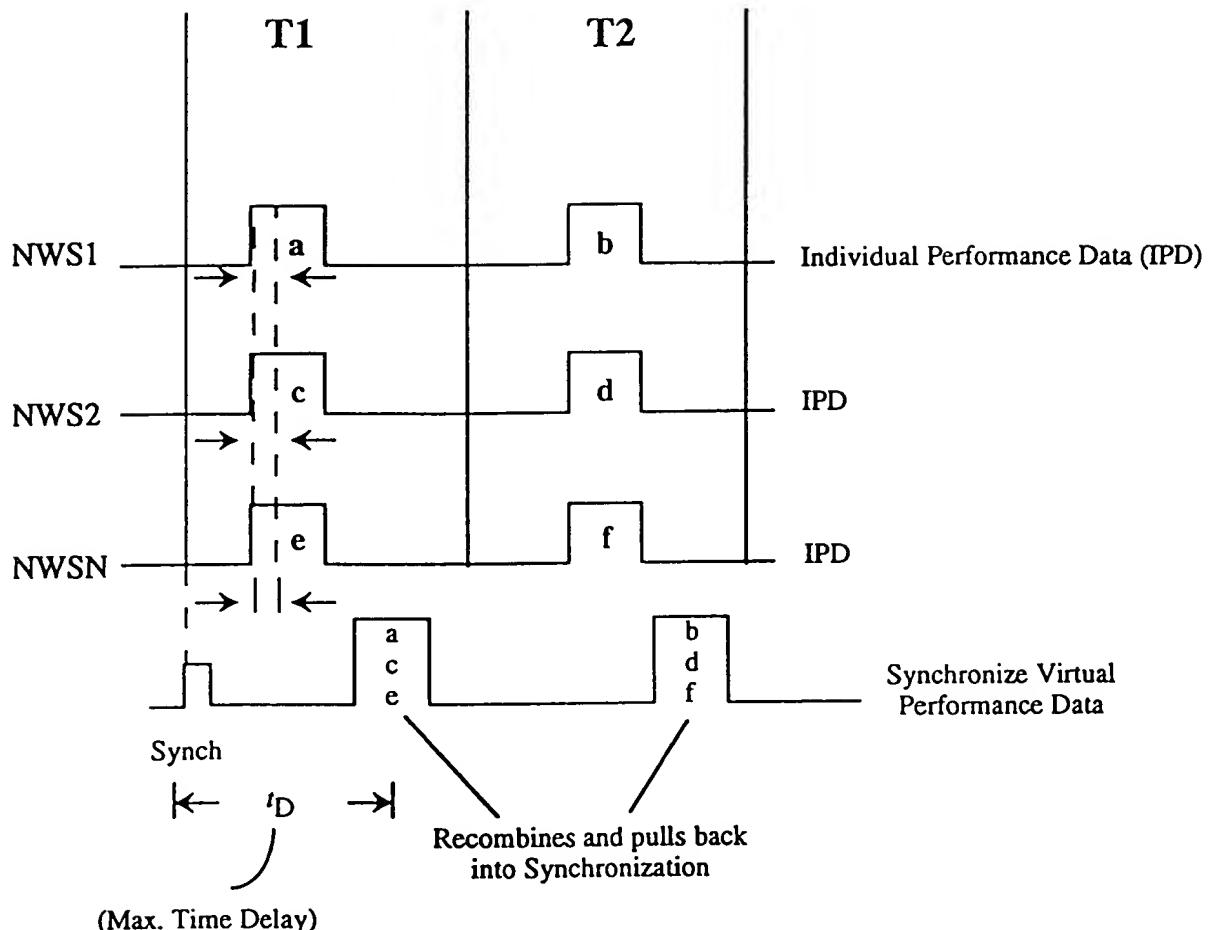
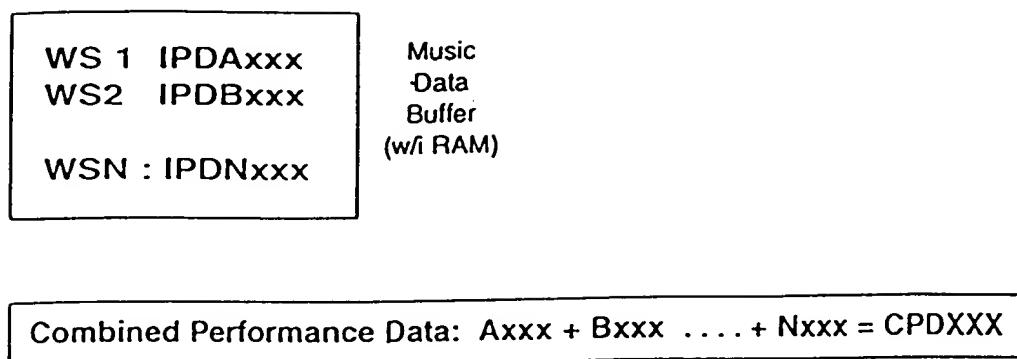


Fig. 18

a, b, c, d, e, f, = data and timing synch info

Master Station Buffer



Individual Work Station

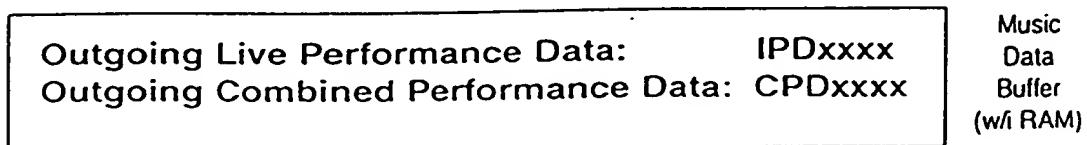


Fig. 19